REMARKS

Claims 10, 11 and 14-16 remain pending. The allowance of claims 10 and 11 is noted with appreciation.

Claims 14-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over patent application publication no. US 2003/0028704 A1 to Mukaida et al. (hereinafter "Mukaida") in view of patent application publication no. US 2004/0030825 A1 to Otake et al. (hereinafter "Otake").

Claim 14 recites writing data in one of two different ways, depending upon the amount of data that are received with a write command:

(1) If the amount of data for a *plurality of pages* are received, the operation comprises "writing all the received data in parallel into pages within a plurality of blocks of *at least one of the metablocks in a plurality of the sub-arrays*." (Emphasis Added.)

(2) If the amount of data for *only a single page* are received, the operation comprises "writing all the received data in parallel into *individual pages of individual blocks of only one of the sub-arrays*." (Emphasis Added.)

This combination takes advantage of a high degree of parallelism (feature (1) above) but recognizes the disadvantages of operating with a high degree of parallelism (feature (2) above) when only a single page of data are to be written into the memory. (See paragraph 0012 of the present application, for example, for a summary.) By use of feature (2) above, there is a reduction of the number and frequency of garbage collection operations that become necessary to combine small amounts of valid data in order to allow erasing the blocks in which such small data amounts are stored. But, at the same time, the advantages in speed of multi-page parallel data writing are maintained (feature (1) above) in situations where the single page write disadvantages do not exist.

The Office Action contends (page 3, lines 16-20; page 6, lines 6-13) that writing data into pages of "only one of the sub-arrays" (feature (2) above) is described by Mukaida (Figure 22, and paragraphs 0289-0297 and 0344-0346). The Office Action (page 4, lines 2-12) also contends that writing data into "at least one of the metablocks in a plurality of the sub-arrays" (feature (1) above) is not disclosed by Mukaida but rather is described by Otake (paragraphs 0036-0051). It is then alleged (Office Action, page 4, lines 14-21) that it would have been

obvious for a person of ordinary skill to combine these two operational features in a single memory system.

Assuming for the purpose of argument that these characterizations of Mukaida and Otake are correct, this position of obviousness is respectfully traversed. There is certainly nothing cited in either Mukaida or Otake that might suggest such a combination. Claim 14 defines the use of one writing technique in response to the receipt of one quantity of data with a write command, and the second writing technique in response to the receipt of another quantity of data with a write command. This particular combination of techniques is designed to optimize performance of the memory system. It is very important to distinguish this from the case where it might be argued that Otake would have made it obvious to change the way Mukaida writes data in total. Whatever may be said for that position does not apply to the present case, where the both of the data writing techniques alleged in the Office Action to be described by Mukaida and Otake are being used in a single memory system in response to different types of data commands (1) and (2) recited above. No reason can be imagined by one of ordinary skill would have thought to combine the different writing operations of Mukaida and Otake under the specific circumstances claimed, namely whether a plurality of pages or a single page of data are received with a write command. Neither Mukaida nor Otake are seen to even suggest any limitations of their methods, the limitations of which are recognized in the compromise defined by claim 14 that includes the two write methods (1) and (2) quoted above. It is therefore submitted that it would not have been obvious from Mukaida and Otake to form such a specifically claimed combination of data write operations.

The Office Action (page 4, lines 20-21) gives as a reason why such a combination would have been obvious, "because it improves the performance of writing in flash memories by decreasing evacuation [garbage collection] in rewriting." But nothing in Mukaida and Otake can be found to suggest such a reason. That reason might provide a basis for arguing the obviousness of changing the way Mukaida operates to that of Otake but this is quite different than what is defined by claim 14. Claim 14 does not just define a memory system of one reference that has its operation changed in accordance with the teachings of another reference. Both of the data writing techniques attributed in the Office Action to Mukaida and Otake are used together in a way and for reasons not suggested by either of the references. It is therefore

respectfully submitted that the Office Action does not provide any reasonable basis to conclude that it would have been obvious to combine the teachings of the references to result in the detailed memory system operation including features (1) and (2) of claim 14 discussed above.

Further, contrary to what is assumed in the foregoing discussion for the purpose of responding to the obviousness arguments of the Office Action, it is respectfully submitted that assertion in the Office Action (page 3, lines 16-20) that Mukaida (Figure 22, paragraphs 0289-0297 and 0345-0346) describes feature (2) above is contrary to what is described in Mukaida. The rejection appears to now be based on the description in paragraphs 0345-0346 of Mukaida, which describe storing multiple pages of data on a single memory chip. But it should be noted that the multiple pages of data written to each of the flash memory chips 32-3 and 32-2 are written to different blocks of memory cells on those chips. As shown in Figure 23, the blocks of these two memory chips are each divided into four banks ##0-3. The description of paragraphs 0345-0346 appears to be directed to writing data in all four banks of one chip at the same time, with the blocks to which the data are being written being in different banks. The timing diagram of Mukaida's Figure 29 shows the parallel writing of data into banks ##0-3 of chip 32-3, and then parallel writing of data into banks ##0-3 of chip 32-2. Paragraph 0346 describes the advantage of this to be that parallel data writing can exist in a single chip by dividing it into multiple banks of memory cell blocks.

What is clear is that the cited paragraphs 0289-0297 and 0345-0346 of Mukaida, and accompanying timing diagrams of Figures 22 and 29, do not describe writing single pages of data received with a write command into a single bank. Claim 14, and thus also its dependent claims 15 and 16, are therefore respectfully submitted to be patentable for this additional reason.

Yet another feature believed to be novel over the cited references is recited in the "maintaining indications" limitation of the last paragraph of claim 14. The Office Action (page 3, line 20 – page 4, line 1) contends that this feature is disclosed by Mukaida (citing paragraphs 0275-0278). But those paragraphs describe Figure 20 that illustrates an internal translation of addresses during the reading of data from the memory. Claim 14, on the other hand, defines operating the memory system to write data in response to received write commands, including maintaining indications associated with the written data of whether the data received with a write command have been "into one of either (1) a single block or (2) a plurality of blocks of a

metablock." It is simply not understood how the cited portions of Mukaida can be said to describe this.

In the Response to Arguments portion of the Office Action (paragraph bridging pages 6 and 7), the alternative language of the "maintaining indications" limitation of the last paragraph of claim 14 appears to have been interpreted to define the overall operation recited in the claim. But the alternative language at the end of claim 14 is clearly limited to the "maintaining indications" feature of the last claim paragraph, and does not limit the overall operation that is earlier defined by the claim. And as to "maintaining indications," the alternative language at the end of the claim is being amended to make clearer that the memory system operates to maintain both of the recited indications. One of the recited indications is maintained for a given data write, depending on its characteristics.

Conclusion

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. However, if the Examiner has any further matters that need to be resolved, a telephone call to the undersigned attorney at 415-276-6534 would be appreciated.

FILED VIA EFS

Respectfully submitted,

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